provided for coins and bills) is connected to the input interface circuit group **62**, and when a coin is inserted into the aforementioned coin insertion slot **44**, or when a bill is inserted into the bill insertion slot **46**, then insertion information relating to the types and number of the inserted coins or bills is supplied.

[0080] Moreover, a touch panel **28** is connected to the input interface circuit group **62**, and information indicating the contact position on the touch panel **28** is read in appropriately.

[0081] The CPU **66** described above switches processing, and the like, as appropriate, in accordance with input information, and the like, from the input interface circuit group **62**.

[0082] The speakers **80**, indication lamp **56** and pay-out device **82** are connected to the output interface circuit group **72**, and the interface circuit group **72** drives and controls the speakers **80**, indication lamp **56**, pay-out device **82**, and the like, under the control of the CPU **66**.

[0083] Furthermore, a display control device **200** is also connected to the output interface circuit group **72**, and the display control device **200** controls the main display device **32**, and the first to third sub display devices **34**, **36** and **38**, on the basis of an image display command issued by the main control circuit **60**. The display control device **200** is installed on a circuit board (not limited to being only one circuit board), which is different from the circuit board on which the main control circuit **60** is installed.

[0084] (Composition of Display Control Device in Game Selection-Enabled Gaming Machine)

[0085] **FIG. 5** is a block diagram showing the detailed composition of the display control device **200**.

[0086] In **FIG. 5**, the display control device **200** comprises a CPU **206**, a ROM **208**, a RAM **210**, an interface circuit **202**, a video display processor (VDP) **212**, a video RAM **214**, an image data ROM **216**, and four display drive circuits **218**, **220**, **222** and **224**; the CPU **206**, ROM **208**, RAM **210**, interface circuit **202** and video display processor **212** are connected to the input/output bus **204**, and the video RAM **214**, image data ROM **216**, and four display drive circuits **218**, **220**, **222** and **224** are connected to the video display processor **212**.

[0087] The interface circuit **202** receives and processes image display commands, and the like, from the main control circuit **60** described above, and supplies these commands to the CPU **206**, via the input/output bus **204**.

[0088] The CPU **206** executes the display control program stored in the ROM **208**, on the basis of the image display command thus supplied, using the RAM **210** as a working memory, and it instructs the video display processor **212** to carry out the actual image display processing. Here, the data, and the like, required for display control which forms one part of the game program is stored in the RAM **210**. The ROM **208** and RAM **210** may be other storage media.

[0089] The video display processor **212** includes circuits, such as a so-called sprite circuit, screen circuit and palette circuit, and the like, which carry out various image processing for displaying images on the main display device **32** and the first to third sub display devices **34**, **36** and **38**; Here, the

game images are displayed on the main display device **32**. A video display processor (VDP) may be provided separately for the each of the main display device **32** and first to third sub display devices **34**, **36** and **38**.

[0090] The video RAM **214**, which stores image data in accordance with image display command issued by the main control circuit **60**, and the image data ROM **216**, which stores image data, such as image data for a background, image data for symbols, image data for characters, and the like, are connected to the video display processor **212**. The display drive circuits **218**, **220**, **222** and **224** which drive the main display device **32** and the first to third sub display devices **34**, **36** and **38** are also connected to the video display processor **212**.

[0091] The CPU **206** stores the image data to be displayed on the main display device **32**, in the video RAM **214**, in accordance with the image display command issued by the main control circuit **60**, by reading out and executing a display control program stored in the ROM **208**. The image display commands issued by the main control circuit **60** include display commands such as a background display command, a symbol display command, a character display command, and the like.

[0092] Furthermore, as described above, the image data ROM **216** stores image data for a symbol image, which is an identification information image, character image data for a character, such as a moving object displayed as an effect screen, and background image data forming the background of the main display device **32**, and the like.

[0093] The symbol image data described above is used when symbols are variably displayed on the main display device **32**, or when symbols are stopped and displayed, and it includes image data according to various different display modes, such as enlarged images, reduced images, modified images, and the like. Furthermore, the character image data described above includes image data required in order to display a mode where a character performs a sequence of actions.

[0094] **FIG. 6** is a schematic drawing illustrating the concept of image data generated in the aforementioned video RAM **214**.

[0095] As shown in **FIG. 6**, the size of the image data generated in the video RAM **214** in accordance with the image display command (hereinafter, called the "screen image region" R1) is set to be greater than the display region R2 shown on the main display device **32**. In **FIG. 6**, the screen image region R1 is the region demarcated by the solid line and the display region R2 is the region demarcated by the broken line. By setting the size of the image data in this way, it is possible to provide a smoothly scrolling display of the image that is to be shown on the main display device **32**.

[0096] If a symbol display command is issued by the main control circuit **60**, then the video display processor **212** reads out the image data for the respective images D1 to D3 showing symbols which are identification information images, from the image data ROM **216**, and it then situates the image data thus read out in a position in the video RAM **214** which corresponds to the position at which the symbol image is to be displayed on the main display device **32**. Furthermore, if a character display command is issued by the main control circuit **60**, then the video display processor **212**